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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/850,254	05/07/2001	Hisamitsu Kimoto	N13476100S	1494

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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/850,254	KIMOTO, HISAMITSU	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondenc address* --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

2. Therefore, the "first wiring trace in the second wiring region disposed in the second direction; a second wiring trace in the second wiring region disposed in the second direction and separated from the first wiring trace in the first direction; and a third wiring trace in the first wiring region disposed in the first direction and electrically connecting the first wiring trace and the second wiring trace" in **claim 4** must be shown or the features canceled from the claim.

3. The "memory array having bit lines formed with a second wiring layer" in **claim 5** must be shown or the features canceled from the claim. No new matter should be entered.

4. The "dynamic random access memory cells having a capacitor over bit line structure" in **claim 6** must be shown or the features canceled from the claim. No new matter should be entered.

5. The "plurality of functional circuit blocks are disposed in a matrix on the surface of a semiconductor substrate" in **claim 11** must be shown or the features canceled from the claim. No new matter should be entered.

6. The "memory array having bit lines formed with a second wiring layer" in **claim 12** must be shown or the features canceled from the claim. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The examiner believes that neither the specification nor the figures disclose the subject matter of claim 4.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "first wiring layer" in claims 1 and 7 are used by the claims to mean "M2," while the accepted meaning is "M1." In the semiconductor art, the first wiring layer or metal 1 or "M1" is the first wiring layer which is formed over the substrate and *therefore the lowermost wiring layer* (closest to the substrate). The applicant's specification discloses that "M2" has vertical track wiring region and a horizontal track wiring region (p. 9, lines 10-15). In this case, the applicant has utilized "M2" in its known definition, which is metal 2 or the second wiring layer. In the semiconductor art, the second wiring layer is *above* the first wiring layer because it is *formed after the first wiring layer*. The examiner believes that the intent of the applicant was to claim a device with at least two wiring layers where the second wiring layer or "M2" or metal 2 layer has a vertical track wiring region and a horizontal track wiring region. The examiner is not sure if this was the intent of the applicant and has therefore accordingly interpreted "a first wiring layer" in claims 1 and 7 (and therefore claims 4-6 and 8-13) and "a second wiring layer" in claims 3 and 9 (and therefore claims 4-6 and 10-13) *to include any two different wiring layers, regardless of whether or not it is actually a first wiring layer or a second wiring layer.*

13. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. Claim 11 is further rejected under 35 U.S.C. 112, second paragraph because of the phrase "the plurality of functional circuit blocks are disposed in a matrix on the surface of a

semiconductor substrate." The claim refers to a "matrix" which is also referred to in the specification as a "matrix configuration," but "the plurality of functional circuit blocks are disposed in a matrix on the surface of a semiconductor substrate" is never illustrated. Therefore the examiner is not certain of the metes and bounds of the phrase "the plurality of functional circuit blocks are disposed in a matrix on the surface of a semiconductor substrate." This claim is therefore rendered indefinite.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

16. Claims 1, 2, 7, 8, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Hiraga (USPN 6,064,097).

17. So far as understood in claims 1 and 2, Hiraga (USPN 6,064,097) discloses a similar device. Figure 5 of Hiraga illustrates a semiconductor apparatus with a plurality of device elements (30) formed on the surface of the semiconductor substrate (not labeled). Each device element (30) has a diffusion region (36 and the rectangular areas which are indicated with a doping of N+ and P+). A first wiring layer is part of a multi-layer wiring configuration which provides an electrical connection between two diffusion regions (36 and the rectangular areas

which are indicated with a doping of N+ and P+). The signal lines (not labeled, but are the bold lines in figure 5) are a part of the first wiring layer. The signal lines (not labeled but are the bold lines in figure 5) meet claims 1 and 2. Several of the signal lines have a first wiring region which is parallel to the V_{DD} line. This is a first wiring direction. Figure 5 also illustrates that several of the signal lines have a second wiring region which is perpendicular to the V_{DD} line. This is a second wiring direction and therefore meets the limitation of claim 2. One of the signal lines provides an electrical connection between a diffusion region (36) in the PMOS section (34 or the upper half of the figure) and a diffusion region (36) in the NMOS section (the lower half of the figure). This signal line is the rightmost bold line in figure 5.

18. So far as understood in claims 7 and 8, Hiraga discloses a similar device. Figure 5 of Hiraga illustrates a semiconductor apparatus with a functional circuit block. It is understood that the functional circuit block of figure 5 is duplicated many times on the semiconductor substrate. The functional circuit blocks has a plurality of device elements (30) formed on the surface of the semiconductor substrate (not labeled). Each device element (30) has a diffusion region (36 and the rectangular areas which are indicated with a doping of N+ and P+). A first wiring layer is part of a multi-layer wiring configuration which provides an electrical connection between two diffusion regions (36 and the rectangular areas which are indicated with a doping of N+ and P+). The signal lines (not labeled, but are the bold lines in figure 5) are a part of the first wiring layer. The signal lines (not labeled but are the bold lines in figure 5) meet claims 7 and 8. Several of the signal lines have a first wiring region which is parallel to the V_{DD} line. This is a first wiring direction. Figure 5 also illustrates that several of the signal lines have a second wiring region which is perpendicular to the V_{DD} line. This is a second wiring direction and therefore meets the

limitation of claim 8. One of the signal lines provides an electrical connection between a diffusion region (36) in the PMOS section (34 or the upper half of the figure) and a diffusion region (36) in the NMOS section (the lower half of the figure). This signal line is the rightmost bold line in figure 5.

19. So far as understood in claim 12, Hiraga meets the limitation of the claim. The rightmost bold line in figure 5 illustrates a signal line in the first wiring layer. As discussed above, this particular signal line provides an electrical connection between a diffusion region or source/drain region (36) in the PMOS section (34 or the upper half of the figure) and a diffusion region or source/drain region (36) in the NMOS section (the lower half of the figure). Both of the diffusion regions or source/drain regions have two gate electrodes for insulated gate field effect transistors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
March 9, 2002